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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,171	12/19/2000	Steven Teig	SPLX.P0017	8567

23349 7590 05/21/2004

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,171	TEIG ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-31,34-36,39-46,49-51 and 54-57* is/are rejected.

7)☒ Claim(s) *32, 33, 37, 38, 47, 48, 52, 53, 58-75* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. 01/29/2004; 03/03/2004; 10/10/2003; 03/03/2004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment and Response to Office Action has been reviewed and examined. Claims 28, 30, 32, 43, 45, 47, 58, and 67 are amended. Claims 28-75 are pending.

1. Applicant's Amendment is persuasive-in-part and obviates some objections of the prior office action. The pertinent rejection of the prior office action are incorporated herein.

Claim Objections

2. Claims 38 and 53, are objected to because of the following informalities: Pursuant to claims 38 and 53, "said slots" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

4. A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 28-31, 34-36, 39-46, 49-51 and 54-57

5. Claims 28-31, 34-36, 39-46, 49-51 and 54-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Rostoker et al. (Rostoker), U.S. Patent 5,822,214.

Rostoker discloses cell architecture using hexagonal shaped cell and CAD methods relating to this type of architecture.

6. Pursuant to claim 28, Rostoker discloses a method of placing circuit modules in a region of an integrated circuit layout (col. 42, ll. 26-47 discloses floorplanning and placement) the method comprising partitioning the IC regions into several sub-regions, wherein a plurality of edges exist between said sub-regions, wherein a plurality of said edges are diagonal (col. 42, ll. 8-25 discloses partitioning; col. 41, ll. 55-65 discloses diagonal (or sixty degree edges); (see also col. 42, ll. 58-62); see also floorplanning and placement (col. 51, line 25 – col. 56, line 56);

selecting a net (col. 42, ll. 58-62);

identifying the set of sub-regions containing the circuit elements of the selected net;

identifying the edges, from the plurality of edges, intersected by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified edges is diagonal (col.. 42, ll. 48-58; col. 56, line 56 to col. 59, line 63;

computing a placement cost by using the identified edges (col. 59, ll. 41-64).

7. Pursuant to claim 29, wherein a plurality of said edges are horizontal and a plurality are vertical (col. 41, ll. 58-64).

8. Pursuant to claim 30, wherein partitioning the IC region comprises using a set of partitioning lines to define sub-regions (col. 42, ll. 8-25).

9. Pursuant to claim 31, wherein the plurality of edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines (col. 58, line 36 to col. 59, line 65).

10. Pursuant to claim 34, further comprising changing the position of a circuit element of the selected net from one sub-region to another; identifying a new set of sub-regions that contain the elements of the selected net; identifying a new set of edges intersected by at least one new connection graph; computing a new placement cost by using the identified new set of edges (col. 60, line 11 to col. 61, line 36).

11. Pursuant to claim 35, further comprising for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net; identifying a set of edges intersected by at least one connection graph that represents the topology of one or more interconnect lines (col. 59, ll. 5-63); computing a placement cost for the IC layout within said region based on the identified set of edges.

12. Pursuant to claim 36, further comprising changing the position of a particular circuit element from one sub-region to another; for each particular net that includes the element, identifying the sub-regions that contain the circuit elements of the particular net. . .computing a placement cost (col. 60, line 11 to col. 61, line 36).

13. Pursuant to claim 39 wherein identifying the edges comprises identifying the edges intersected by all optimal connection graphs for the selected net (col. 59, ll. 54-63).

14. Pursuant to claim 40 wherein the connection graphs are determined to be optimal based on at least one particular selection criteria (col. 59, ll. 5-63).

15. Pursuant to claim 41, wherein the selection criterion is the length of the connection graph (col. 58, line 44 to col. 59, line 63).

16. Pursuant to claim 42, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs (col. 57, line 7 to col. 59, line 21).

17. Pursuant to claims 43-46, 49-51, and 54-57, these claim incorporate similar limitations to claims 28-31, 34-36, and 39-42, already rejected supra, and therefore claims 43-46, 49-51, and 54-57 are likewise rejected based on the same reasoning.

Allowable Subject Matter

18. Claims 32, 33, 37, 38, 47, 48, 52, 53 and 58-75 contain allowable subject matter.

19. The following is a statement of reasons for the indication of allowable subject matter: In a method of placing circuit modules involving diagonal edges and line paths, the prior art does not disclose an octagonal wiring model that has forty-two edges. Further, the prior art does not disclose storing a plurality of identified edges or line paths in a storage structure.

Remarks

20. Rostoker anticipates Applicant's invention. Examiner has provided specific cites in Rostoker for each of the limitations. Examiner has provided cites in Rostoker for diagonal line paths that exist between the sub-regions (Fig. 91; col. 6, ll. 48-53; col. 19, ll. 1-4, in addition to the cites provides, supra) and cites where Rostoker discusses identifying line paths used by a connection graph (the Steiner tree, col. 59 ll. 54-59) and cites that disclose computation of placement cost by using identified line paths (col. 44,

ll. 59-62; col. 59, ll. 29-48; col. 59, ll. 60-63). The connection graphs and line graphs claimed by Applicants represent nothing more than Steiner trees and Rostoker discloses Steiner tree algorithms for three directional (including diagonal) routing.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562 or the Customer Service Center whose telephone number is (571) 272-1750.

23. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner
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